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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/019,406	12/28/2001	Takanori Shimura	520.41005X00	3912

20457 7590 12/23/2004

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EXAMINER	
HENRY, MATTHEW ALLAN	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/019,406	SHIMURA ET AL.	
	Examiner	Art Unit	
	Matthew A. Henry	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-7,10 and 12-14* is/are rejected.

7)☒ Claim(s) *2,3,8,9 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/28/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

On Pages 27, Lines 7-9, the specification reads "three kinds of high frequency, middle frequency and low frequency." It should read "three frequencies: high frequency, middle frequency and low frequency."

On Pages 28, Lines 1, the word "incosistent" should be replaced with "inconsistent" to be correct.

On Page 32, Line 25, the specification reads "three kinds of a high frequency . . ." It should read "three frequencies: a high frequency . . ."

Appropriate correction is required.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 4 recites the limitation "said clock control signal" in Paragraph 2, Line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim because a clock control signal has not been previously recited in Claim 4 or in Claim 1, from which Claim 4 depends.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4, 5, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mittal in view of Tran.

Regarding Claim 1, Mittal discloses:

A semiconductor device (Figure 5, Item 500) comprising:

a plurality of functional units (Figure 5, Items 501-504; Column 10, Lines 64-67) connected to each other by an internal bus (though not specifically listed, the internal bus is inherent to the system shown in Figure 5),

operation mode outputting means provided to each of said plurality of functional units (Figure 1, Item 109; Column 5, Lines 31-32) outputting a request of changing an operation mode at a frequency in operation to other operation mode (Column 5, Lines 22-24) in accordance with a data processing content (Figure 1, Item 108; Column 5, Lines 18-20), and

power-execution controlling means (Figure 1, Item 107; Column 5, Lines 25-29) controlling a frequency of a clock signal (Column 7, Lines 27-28) used by the functional unit executing a processing so that a total of power consumption functional executing the processing in said plurality of functional units does not exceed a limit of power consumption provided to the semiconductor device (Column 4, Lines 61-63) in accordance with said request of changing the operation mode.

Mittal does not, however, disclose controlling the power consumption of the device by adjusting a bus operation time.

Tran teaches:

Preventing bus signals from switching except when true data have arrived to cut down the unnecessary power dissipation (Column 3, Lines 18-20).

Tran demonstrates that power consumption can be controlled in the additional method of adjusting bus operation. Adjusting the bus access time of a functional unit and adjusting the clock frequency of the functional unit are functionally exclusive methods for controlling the power consumption of the functional unit. Because of this distinction, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Mittal to further incorporate a bus operation controlling method as described by Tran to provide further control over the power consumption of the device.

Regarding Claim 4, Mittal and Tran further teach:

each of said plurality of functional units includes;

clock selecting means for selecting a clock signal (Figure 2, Item 203; Column 8, Lines 27-32, 35-40 and 49-53) having a corresponding frequency from the plurality of clock signals by receiving said clock control signal (Figure 2, Item 204; Column 8, Lines 42-43), and data processing means operating with the selected clock signal (Figure 2, Item 206).

Mittal does not disclose:

setting a transfer speed of data transmitted to the bus in accordance with the bus operation time control signal.

According to Tran's teachings, however, it would have been obvious to a person of ordinary skill in the art to provide a means of setting a transfer speed of data transmitted to the bus so as to provide a means for affecting the bus operation time.

Regarding Claims 5 and 12, Mittal further discloses:

said power-execution controlling means includes means for detecting a change of the operation mode in said request of changing the operation mode (Figure 1a, Item 107; Column 5, Lines 22-24) and starts an operation of controlling the frequency of the clock signal and the bus operation time at a time point of detecting any change of the operation mode of the functional unit executing the processing (Column 5, Lines 22-29; the mode controller generates a mode control signal which switches the power mode operation of the functional unit; Column 7, Lines 27-28; the power mode can be affected by adjusting the clock rate of the functional unit).

Mittal does not disclose starting the operation of controlling the bus operation time at a time point of detecting any change of the operation mode of the functional unit executing the processing.

Tran teaches of adjusting the bus operation time to save power (Column 3, Lines 18-20).

Although Mittal does not disclose of adjusting both of these elements according to power mode, it would have been obvious to a person of ordinary skill in the art to combine Tran and Mittal as described above in Claim 1 such that the bus operation time and the clock frequency would both be adjusted at the time point of a detected change in operation mode to maximize the power saved.

Regarding Claim 10, Mittal discloses:

A semiconductor device (Figure 5, Item 500) comprising:

a plurality of functional units (Figure 5, Items 501-504; Column 10, Lines 64-67) connected to each other by an internal bus (though not specifically listed, the internal bus is inherent to the system shown in Figure 5), and a power-execution control circuit (Figure 1, Item 107; Column 5, Lines 25-29) for controlling and setting a frequency of a clock signal (Column 7, Lines 27-28) used by the functional unit executing a processing so that a total of power consumption of the functional unit executing the processing in said plurality of functional units does not exceed a limit of power consumption provided to the semiconductor device (Column 4, Lines 61-63) and outputting a clock control signal for causing the functional unit executing the processing to operate at the set frequency of clock signal (Figure 1a, Item 110),

wherein each of plurality of functional units includes; a clock selector for selecting the clock signal of a corresponding frequency from the plurality of clock signals (Figure 2, Item 203; Column 8, Lines 27-32, 35-40 and 49-53) by receiving the clock control signal (Figure 2, Item 204; Column 8, Lines 42-43),

a data processing circuit operating with the selected clock signal (Figure 2, Item 206), and

an operation mode output circuit (Figure 1, Item 109; Column 5, Lines 31-32) for outputting a request of changing an operation mode at a frequency in operation to other operation mode (Column 5, Lines 22-24) in accordance with a data processing content (Figure 1, Item 108; Column 5, Lines 18-20), and wherein said power-execution control circuit generates and outputs said clock control signal in accordance with said request of changing the operation mode

(Column 5, Lines 22-29; the mode controller generates a mode control signal which switches the power mode operation of the functional unit; Column 7, Lines 27-28; the power mode can be affected by adjusting the clock rate of the functional unit).

Mittal does not disclose:

Controlling and setting a bus operation time used by the functional unit,

A bus operation time control signal to enable the set bus operation time,

setting a transfer speed of data transmitted to the bus in accordance with the bus operation time control signal.

said power-execution control circuit generates and outputs said bus operation time control signal in accordance with said request of changing the operation mode

Tran teaches:

Preventing bus signals from switching except when true data have arrived to cut down the unnecessary power dissipation (Column 3, Lines 18-20).

Tran demonstrates that adjusting bus operation can also control power consumption. Mittal states, "[Our] invention is flexible in that it encompasses a wide range of design alternatives for reducing the power of the functional unit that it controls" (Column 7, Lines 21-23).

Adjusting the bus access time of a functional unit and adjusting the clock frequency of the functional unit are functionally exclusive methods for controlling the power consumption of the functional unit. Because of this distinction, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Mittal to further incorporate a bus operation controlling method as described by Tran to provide further control over the power

consumption of the device. This method would have mirrored the method used by Mittal to control power consumption by varying the clock speed of the functional unit, thereby including the existence and generation of a bus operation time control signal for the purposes of controlling and setting the bus operation time used by a functional unit and affecting the data transfer to the bus in accordance with this control signal.

6. Claims 6, 7, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mittal in view of Tran and further in view of Durham ('036) and ('826).

Regarding Claims 6 and 13, Mittal and Tran teach:

controls to lower the clock frequency of the functional unit (Column 7, Lines 27-28) so that a total of the calculated power consumption does not exceed the limit of power consumption provided to the semiconductor device (Column 4, Lines 61-63).

Mittal and Tran do not teach:

controls to lower the clock frequency of the functional unit having a low priority of data processing,

said power-execution controlling means includes means for calculating a total of the power consumption of the functional unit executing the processing.

Durham ('826) teaches:

said power-execution controlling means includes means for calculating a total of the power consumption of the functional unit executing the processing (Figure 2, Item 230; Column 3, Lines 26-31).

Durham ('036) teaches:

controls to lower the clock frequency (Column 6, Lines 21-23) of the functional unit having a low priority of data processing (Columns 5 and 6, Lines 17-22 and Lines 15-17, respectively; a functional unit with higher priority would be a less suitable target)

Durham provides as motivation for both of his teachings by stating, "Limiting power dissipation is one of the major goals when designing a microprocessor" (Column 1, Line 12).

Accordingly, at the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the teachings of Mittal and Tran with the teachings of Durham so that the power consumption may be measured in individual functional units and controlled in a more accurate manner.

Regarding Claims 7 and 14, Mittal and Tran do not teach:

voltage detecting means for detecting a voltage of power source used internally,

wherein said power-execution controlling means calculates a total of the power consumption of the functional unit executing said processing by the voltage detected by using said voltage detecting means.

Durham teaches:

voltage detecting means for detecting a voltage of power source used internally (Figure 2, Item 230; Columns 3 and 5, Lines 26-27 and 1-5, respectively),

wherein said power-execution controlling means calculates a total of the power consumption of the functional unit executing said processing by the voltage detected by using said voltage detecting means (Column 3, Lines 28-31).

Durham provides as motivation by stating, "Limiting power dissipation is one of the major goals when designing a microprocessor" (Column 1, Line 12).

Accordingly, at the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the teachings of Mittal and Tran with the teachings of Durham so that the power consumption may be measured in individual functional units and controlled in a more accurate manner.

Allowable Subject Matter

7. Claims 2, 3, 8, 9 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claims 2, 3, 8 9 and 11, the following limitations cannot be met by prior art:

means for storing information with regard to the power consumption, the individual bus operation time and a priority of data processing for respective operation modes of said plurality of functional units, and

means for assigning the power consumption and the individual bus operation time to the functional unit executing said processing successively from the functional units having higher priorities of data processing by using said information.

Shaffer teaches of a memory (Figure 1, Item 26) that stores a table (Figure 1, Item 28; Column 3, Line 26) that may be used to store information regarding a CPU's operating

requirements (Column 3, Lines 39-41). Shaffer further teaches a clock speed being assigned to the CPU according to the information stored in the table (Column 4, Lines 40-46).

While it may have been obvious to combine the teachings of Shaffer with a method for controlling the bus operation and the clock frequency of a number of functional units based upon the priorities associated with each functional unit and the activity of each functional unit, it would not have been obvious to a person of ordinary skill in the art to combine the teachings of Shaffer with the teachings of Mittal and Tran because it would have substantially changed the methodology used to implement the device described specifically by Mittal.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew A. Henry whose telephone number is (571) 272-3845. The examiner can normally be reached on Monday - Friday (8:00 am -5:00 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MAH

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